REMARKS

The present application was filed on December 18, 2001 with claims 1 through 22. Claims 3-6, 11, 13 and 14 were previously cancelled herein, without prejudice, and claims 23 through 29 were previously added. Claims 1, 2, 7-10, 12 and 15-29 are presently pending in the above-identified patent application. Claim 16 is proposed to be amended herein

In the Office Action, the Examiner rejected claims 8, 9, 15 and 27-29 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 16-22 were rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. The Examiner rejected claims 16-19 and 22 under 35 U.S.C. §103(a) as being unpatentable over Raghavan (United States Patent No. 6,418,172) in view of Trans (United States Patent No. 6,377,640). In addition, the Examiner rejected claims 1, 7, 8, 12, and 15 under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of "A Low Complexity Joint Equalizer and Decoder for 1000 Base-T Gigabit Ethernet" (Haratsch 1). The Examiner rejected claim 20 under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans, and further in view of Haratsch 1. Claims 2, 9, 10 and 23-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Haratsch 1 and further in view of "High Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T" (Haratsch 2).

Section 112 Rejection

Claims 8, 9, 15 and 27-29 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner asserts that claim 8 is a "single means claim." (i.e., where a means recitation does not appear in combination with another recited elements of means), and as such is subject to an undue breadth. (citing *In re Hyatt*).

Claim 8, however, is not a single means claim at all. Rather, claim 8 recites a specific structural element (i.e., a sequence detector). As clear from Section 112, Paragraph 6, a "means" recitation is clearly contrasted from a recited structure. Thus, Applicants strongly submit that Hyatt is not at all applicable to the present invention, as recited by claim 8. The

court in Hyatt was considering a claim directed to a Fourier transform processor, comprising "incremental *means*..." There is no "means" recitation in claim 8.

Thus, Applicants respectfully request the withdrawal of the rejection of Claims 8, 9, 15 and 27-29 under 35 U.S.C. §112, first paragraph.

Section 101 Rejection

Claims 16-22 were rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. The Examiner asserts that claim 16 is directed solely to an abstract idea.

Applicants again re-assert their prior argument that claims 16-22 include a *transformation to a trellis representation of an MLT-3 code that provides a useful, concrete and tangible result*. Nonetheless, in order resolve this issue, Applicants have amended claim 16 to emphasize the practical application of the trellis, namely, to decode MLT-3 coded signals.

Applicant submits that claim 16, as amended, is in full compliance with 35 U.S.C. §101, and accordingly, respectfully requests that the rejection under 35 U.S.C. §101 be withdrawn.

Prior Art Rejections

Claim 16-19

Claims 16-19 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Irans. The Examiner asserts that Raghavan discloses a method for representing an MLT-3 code as a trellis using three signal levels to represent two binary values, the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period; and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values.

The Examiner acknowledges that Raghavan does not disclose that a first binary value substantially always causes a *state transition in said trellis* from a first state to a different state and a second binary value does not cause a *state transition in said trellis*," as required by claim 16.

The Examiner asserts, however, that this feature is shown by Irans. To the contrary, however, Irans teaches that each time a logic "1" is encoded, a transition (equal to an

output value transition) will take place (there is no mention of causing a state transition in a trellis). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col. 61, lines 48-56. Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention.

As asserted in Applicants' prior response, Raghavan discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A). Thus, in Raghavan (for example, Fig.1A), the input value 1 *sometimes* causes a transition into the same state, and sometimes a transition into a different state. Thus, one value does not always lead to a state transition as defined in claim 16.

Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16. *Compare,* the trellis of Raghavan to the MLT- trellis of the present invention.

Thus, Raghaven and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value *substantially always* causes a state transition in said trellis *from a first state to a different state* and a second binary value does not cause a state transition in said trellis," as required by claim 16.

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Haratsch 1.

Regarding claims 1 and 8, the Examiner asserts that Raghavan discloses MLT-3 encoding. The Examiner acknowledges that Raghavan does not disclose decoding a signal received from a dispersive channel causing intersymbol interference comprising generating at least one trellis representing the code and the dispersive channel; and performing joint equalization and decoding of the received signal using the trellis. The Examiner asserts, however, that this feature is shown by Haratsch 1.

In order to establish a *prima facie* case of obviousness, the following three criteria must be met:

> [f]irst, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

M.P.E.P. §2143. Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references.

First, as asserted in Applicants' prior response, MLT-3 codes are not trellis coded modulation (TCM) as described by Haratsch 1. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention.

Furthermore, Haratsch 1 is addressing *four dimensional* TCM codes with 8 states. Thus, the branch metric computations disclosed by Haratsch 1, for example, do not make sense in the context of the present invention. For example, Equations 1 and 2 of Haratsch 1 do not make sense for MLT-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the 1D branch metric to obtain 4D branch metrics for the 4D TCM code, which again does not make sense for MLT-3 codes. See also Figures 2 and 4, where one and four dimensional branch metric units are shown.

In addition, as discussed hereinafter, if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense. While the number of trellis states in Haratsch 1 is equal to the number of TCM code states and therefore equal to 8, whereas in the present invention, the number of trellis states is $4x(2^K)$, where K is the truncated channel memory.

Thus, a person of ordinary skill in the art would not make such a combination.

In addition to providing a different number of states, which suggests away from the combination, the minimum number of states associated with the present invention ($4x(2^K)=4$

for K=0) is lower than Haratsch 1. This is a "surprising result" which is further evidence of non-obviousness.

Dependent Claims

Dependent claims 2, 7, 9-10, 12, 15 and 17-29 were rejected under 35 U.S.C. §§102(e) or 103(a) as being anticipated by or unpatentable over Raghavan, Haratsch 1 and Haratsch 2, alone or in combination.

Claims 2, 7, 9-10, 12, 15 and 17-29 are dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Haratsch 1 and Haratsch 2 (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

With respect to claims 26 and 29, for example, the Examiner asserts that Haratsch 2 discloses that the number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory. (citing page 171). In the passage of Haratsch 2 recited by the Examiner, however, the number of states is given by $Sx(2^{mL})$, where S is the number of TCM code states, m the number of bits that are fed into the TCM encoder, and L is the (full) channel memory. m is defined in Fig.2 of Haratsch 2 for TCM codes, but is undefined for MLT-3 codes, which are different from TCM codes. Significantly, the equation in page 171 of Haratsch 2 uses the channel memory L, while claims 26 and 29 use the truncated channel memory K. Therefore, the equation in page 171 of Haratsch 2 is different and undefined for MLT-3 codes.

Conclusion

All of the pending claims, i.e., claims 1, 2, 7-10, 12 and 15-29, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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